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EXAMINER	
BODDIE, WILLIAM	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/724,211	MIYAZAWA, TAKASHI	
	Examiner	Art Unit	
	WILLIAM L. BODDIE	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-20 and 36-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-20 and 36-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/28/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *JP2001-147659 and translation*.

DETAILED ACTION

1. In an amendment dated, July 1st, 2008, the Applicant amended claims 18-19, 37-40, 42 and 45-46. Currently claims 18-20 and 36-51 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 18-20 and 36-51 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 19-20 and 46-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yumoto (US 6,859,193) in view of Dawson et al. (US 6,229,506) and further in view of Yamagishi et al. (JP 2001-147659A).

With respect to claim 19, Yumoto discloses, a method of driving an electro-optical apparatus (fig. 7), the apparatus including n rows of scanning lines (scanA-B in fig. 7) each including a first subscanning line (scanA1) and a second subscanning line (scanB1), m columns of data lines (data in fig. 7), a plurality of power-supply lines (Vdd in fig. 19; there is a Vdd line for each pixel), and a plurality of unit circuits arranged in n rows and m columns in association with intersections of the scanning lines and the data lines (fig. 7),

each of the plurality of unit circuits including a first transistor (TFT2 in fig. 19) having a first terminal and a second terminal (top and bottom of TFT2 in fig. 19), a capacitor (C in fig. 19) coupled to a first control terminal (gate of TFT2 in fig. 19) of the first transistor, a second transistor (TFT4 in fig. 19) that controls the electrical connection between the first terminal and the capacitor (fig. 19), the second transistor having a third terminal and a fourth terminal (left and right of TFT4 in fig. 19), a third transistor (TFT3 in fig. 19) having a fifth terminal and a sixth terminal (left and right of fig. 19), and an electro-optical element (OLED in fig. 19) connected to the first transistor (fig. 19), one of the plurality of power-supply lines being electrically connected to one of the m columns of data lines (fig. 19), a second electrode of the capacitor (top of C in fig. 19) being connected to one of the m columns of data lines (fig. 19);

and a second control terminal (gate of TFT4 in fig. 19) of the second transistor being coupled to one of the second subscanning lines, (scanB in fig. 19), a third control terminal (gate of TFT3 in fig. 19) of the third transistor being coupled to one of the first subscanning lines (scanA in fig. 19), and the sixth terminal being connected to the one of the m columns of data lines (data in fig. 19),

the method comprising:

a first step of accumulating a data signal supplied via one of the m columns of data lines in the capacitor as a charge while the second transistor and the third transistor are both on (beginning of the frame period in fig. 20a-b), and setting a conduction state of the first transistor according to the data signal (col. 20, line 49 - col. 21, line 8);

a second step of turning off the third transistor and turning on the second transistor (note the second pulse on scanB in fig. 20b), and supplying an amount of charge that causes reduction in the conduction state, set in the first step, of the first transistor (col. 21, lines 22-35); and

wherein, in one frame period, a set operation (writing operation) and a reset operation (extinguishing period) are executed alternately each time a scanning line is selected, the set operation causing the conduction state of the first transistor of each of unit circuits on one row connected to the selected scanning line, among the plurality of unit circuits, to be set according to the data signal, and the reset operation causing the second transistor of each of the unit circuits on one row coupled to the selected scanning line to be turned on to thereby turn off the first transistor (col. 20, line 49 – col. 21, line 35).

Yumoto does not *expressly* disclose that the power-supply lines intersect the m columns of data lines, or that the power-supply lines are connected to the data lines via the capacitor.

Dawson discloses an electro-optical apparatus (fig. 5) comprising, a plurality of power supply lines (VSWP in fig. 4; one for each pixel circuit) that intersect m columns of data lines (data line in fig. 4).

Dawson and Yumoto are analogous art because they are both from the same field of endeavor namely OLED pixel circuitry design.

At the time of the invention it would have been obvious to one of ordinary skill in the art to intersect the data lines with the power supply lines of Yumoto, as taught by

Dawson, for the well-known benefit of saving panel space by not requiring an individual power line to each pixel.

Neither Yumoto nor Dawson expressly disclose connecting the power supply line to the data line via the capacitor.

Yamagishi discloses, an electro-optical apparatus (fig. 7) wherein, a power supply line (Vdd in fig. 1) is connected to a data line (data in fig. 1) via a capacitor (C in fig. 1).

Yamagishi, Yumoto and Dawson are analogous art because they are both from the same field of endeavor namely OLED pixel circuitry design.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the pixel circuit of Yumoto with the pixel circuit taught by Yamagishi.

The motivation for doing so would have been to suppress leakage current (Yamagishi; Problem to be Solved).

With respect to claim 20, Yumoto, Dawson and Yamagishi disclose, a method of driving an electro-optical apparatus according to claim 19 (see above).

Yumoto further discloses, scanning lines on which the set operation is executed and scanning lines on which the reset operation is executed being each selected sequentially from the plurality of scanning lines (col. 11, lines 37-42).

With respect to claim 46, Yumoto discloses, a method of driving an electro-optical device (fig. 7), the device including a plurality of first scanning lines (scanB1-BN in fig. 7), a plurality of second scanning lines (scanA1-AN in fig. 7), a plurality of data lines (data in fig. 7), a plurality of power-supply lines that intersect the plurality of data

lines (Vdd in fig. 19), and a plurality of unit circuits (pixels in fig. 7), each unit circuit including an electro-optical element (OLED in fig. 19), a first transistor having a first gate, a first terminal, a second terminal, and a first channel region formed between the first terminal and the second terminal (TFT2 in fig. 19), and each unit circuit receiving a first scanning signal (fig. 20b) supplied through one first scanning line of the plurality of first scanning lines and a second scanning signal (fig. 20a) supplied through one second scanning line of the plurality of second scanning lines, a second electrode of the capacitor being connected to the one of the plurality of data lines, the method comprising:

setting a conduction state of the first transistor, the setting of the conduction state including a supply of a data signal through one data line of the plurality of data lines, each of (i) a second transistor (TFT4 in fig. 19) that controls an electrical connection between the first terminal and a first gate according to the first scanning signal (fig. 19) and (ii) a third transistor (TFT3 in fig. 19) that is controlled by the second scanning signal being in an on-state during at least a part of a first period in which the supply of the data signal is carried out (figs. 19-20b); and

causing a reduction in the conduction state of the first transistor set by the setting of the conduction state, the second transistor and the third transistor being in an on-state and an off-state, respectively, during at least a part of a second period in which the causing of the reduction in the conduction state is carried out, and the first gate being electrically connected to one power-supply line of the plurality of power-supply lines during at least a part of the second period (figs. 19-20b; col. 20, line 50-col. 21, line 35).

Yumoto does not *expressly* disclose that the power-supply lines intersect the m columns of data lines, or that the power-supply lines are connected to the data lines via the capacitor.

Dawson discloses an electro-optical apparatus (fig. 5) comprising, a plurality of power supply lines (VSWP in fig. 4; one for each pixel circuit) that intersect m columns of data lines (data line in fig. 4).

Dawson and Yumoto are analogous art because they are both from the same field of endeavor namely OLED pixel circuitry design.

At the time of the invention it would have been obvious to one of ordinary skill in the art to intersect the data lines with the power supply lines of Yumoto, as taught by Dawson, for the well-known benefit of saving panel space by not requiring an individual power line to each pixel.

Neither Yumoto nor Dawson expressly disclose connecting the power supply line to the data line via the capacitor.

Yamagishi discloses, an electro-optical apparatus (fig. 7) wherein, a power supply line (Vdd in fig. 1) is connected to a data line (data in fig. 1) via a capacitor (C in fig. 1).

Yamagishi, Yumoto and Dawson are analogous art because they are both from the same field of endeavor namely OLED pixel circuitry design.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the pixel circuit of Yumoto with the pixel circuit taught by Yamagishi.

The motivation for doing so would have been to suppress leakage current (Yamagishi; Problem to be Solved).

With respect to claim 47, Yumoto, Dawson and Yamagishi disclose, the method according to claim 46 (see above).

Yumoto further discloses, the first transistor being turned off during at least a part of the second period (col. 21, lines 29-32).

With respect to claim 48, Yumoto, Dawson and Yamagishi disclose, the method according to claim 46 (see above).

Yumoto further discloses, a potential of the one power-supply line being set at a first voltage level (Vdd in fig. 19), and

a second voltage level (threshold value of TFT1; col. 21, lines 28-31) different from the first voltage level being applied during at least a part of the second period (fig. 19).

With respect to claim 49, Yumoto, Dawson and Yamagishi disclose, the method according to claim 48 (see above).

Yumoto further discloses, the second voltage being obtained by subtracting a threshold voltage of the first transistor from the first voltage level, or

the second voltage being obtained by adding the threshold voltage of the first transistor to the first voltage level (col. 21, lines 28-32; should also be noted that the pixel circuits are identical and as such will function identically).

With respect to claim 50, Yumoto, Dawson and Yamagishi disclose, the method according to claim 46 (see above).

Yumoto further discloses, a supply of a current to the electro-optical element being stopped during at least a part of the second period (col. 21, lines 22-35).

With respect to claim 51, Yumoto, Dawson and Yamagishi disclose, the method according to claim 46 (see above).

Yumoto further discloses, each of a first set of unit circuits of the plurality of unit circuits connected to a first power-supply line of the plurality of power-supply lines including the electro-optical element of a first color, and

each of a second set of unit circuits of the plurality of unit circuits connected to a second power-supply line of the plurality of power-supply lines including the electro-optical element of a second color (col. 21, lines 36-41).

5. Claims 36 and 41-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yumoto (US 6,859,193) in view of Yamagishi et al. (JP 2001-147659A).

With respect to claim 40, Yumoto discloses, a method of driving an electronic device (fig. 7) including a plurality of first signal lines (scanB1-BN in fig. 7), a plurality of second signal lines (scanA1-AN in fig. 7), a plurality of power-supply lines that intersect the plurality of second signal lines (Vdd in fig. 19), and a plurality of unit circuits (25 in fig. 7), each unit circuit including a capacitor (C in fig. 19), a first transistor having a first gate, a first terminal, a second terminal, and a first channel region formed between the first terminal and the second terminal (TFT2 in fig. 19), and each unit circuit receiving a first signal supplied through one of the plurality of first signal lines (fig. 20a) and a second signal supplied through one of the plurality of second signal lines (fig. 20b), one of the plurality of power supply lines being electrically being electrically connected to

one of the plurality of second signal lines (fig. 19), a second electrode of the capacitor being connected to the one of the plurality of second signal lines (fig. 19), the method comprising:

setting a conduction state of the first transistor, the setting of the conduction state including a supply of the first signal through the one second signal line, each of a second transistor (TFT4 in fig. 19) that controls an electrical connection between the first terminal and a first gate and a third transistor (TFT3 in fig. 19) that is controlled by the first signal being in an on-state during at least a part of a first period in which the supply of the second signal, is carried out (col. 20, line 49 – col. 21, line 7); and

causing a reduction in the conduction state of the first transistor set by the setting of the conduction state, the second transistor and the third transistor being in an on-state and an off-state, respectively during at least part of a second period in which the causing of the reduction in the conduction state is carried out, and the first gate being electrically connected to one power-supply line of the plurality of power-supply lines during at least a part of the second period (figs. 19-20b; col. 21, lines 22-41).

Yumoto does not expressly disclose connecting the power supply line to the second signal line via the capacitor.

Yamagishi discloses, an electro-optical apparatus (fig. 7) wherein, a power supply line (Vdd in fig. 1) is connected to a second signal line (scanB in fig. 1) via a capacitor (C in fig. 1).

Yamagishi and Yumoto are analogous art because they are both from the same field of endeavor namely OLED pixel circuitry design.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the pixel circuit of Yumoto with the pixel circuit taught by Yamagishi.

The motivation for doing so would have been to suppress leakage current (Yamagishi; Problem to be Solved).

With respect to claim 36, Yumoto and Yamagishi discloses, a driving method according to claim 40 (see above).

Yumoto further discloses, an electronic device, wherein a driving method according to claim 40 (see above) is used (col. 25, lines 1-5).

With respect to claim 41, Yumoto and Yamagishi disclose, the method according to claim 40 (see above).

Yumoto further discloses, the first transistor being turned off during at least a part of the second period (col. 21, lines 30-31).

With respect to claim 42, Yumoto and Yamagishi disclose, the method according to claim 40 (see above).

Yumoto further discloses, a potential of the one of the plurality of power-supply lines being set at a first voltage level (Vdd in fig. 19), and

a second voltage level (threshold value of TFT1; col. 21, lines 28-31) different from the first voltage level being applied during at least a part of the second period (fig. 19).

With respect to claim 43, Yumoto and Yamagishi disclose, the method according to claim 42 (see above).

Yumoto further discloses, the second voltage being obtained by subtracting a threshold voltage of the first transistor from the first voltage level, or

the second voltage being obtained by adding the threshold voltage of the first transistor to the first voltage level (col. 21, lines 28-32; should also be noted that the pixel circuits are identical and as such will function identically).

With respect to claim 44, Yumoto and Yamagishi disclose, the method according to claim 40 (see above).

Yumoto further discloses, an electronic element (OLED in fig. 19) being coupled to the first transistor.

With respect to claim 45, Yumoto and Yamagishi disclose, the method according to claim 44 (see above).

Yumoto further discloses, the electronic element being reset during at least a part of the second period (col. 21, lines 33-50).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 18 and 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yumoto (US 6,859,193) in view of Kanatani et al. (US 5,412,297) and Dawson et al. (US 6,229,506) and further in view of Yamagishi et al. (JP 2001-147659A)..

With respect to claim 18, Yumoto discloses, a method of driving an electro-optical apparatus (fig. 7) including n rows of scanning lines (scanA-B in fig. 7) each including a first subscanning line (scanA1) and a second subscanning line (scanB1), m columns of data lines (data in fig. 7), a plurality of power-supply lines (Vdd in fig. 19), and a plurality of unit circuits arranged in n rows and m columns in association with intersections of the scanning lines and the data lines (fig. 7),

each of the plurality of unit circuits including a first transistor (TFT2 in fig. 19) having a first terminal and a second terminal (top and bottom of TFT2 in fig. 19), a capacitor (C in fig. 19) coupled to a first control terminal (gate of TFT2 in fig. 19) of the first transistor, a second transistor (TFT4 in fig. 19) that controls the electrical connection between the first terminal and the capacitor (fig. 19), the second transistor having a third terminal and a fourth terminal (left and right of TFT4 in fig. 19), a third transistor (TFT3 in fig. 19) having a fifth terminal and a sixth terminal (left and right of fig. 19), and an electro-optical element (OLED in fig. 19) connected to the first transistor (fig. 19), a second electrode of the capacitor being connected to the one of the m columns of data lines (fig. 19);

and a second control terminal (gate of TFT4 in fig. 19) of the second transistor being coupled to one of the second subscanning lines (scanB in fig. 19), a third control terminal (gate of TFT3 in fig. 19) of the third transistor being coupled to the one of the first subscanning lines (scanA in fig. 19), and the sixth terminal being connected to the one of the m columns of data lines (data in fig. 19),

the method comprising:

a first step of accumulating a data signal supplied via the one of the m columns of data lines in the capacitor as a charge while the second transistor and the third transistor are both on (beginning of the frame period in fig. 20a-b), and setting a conduction state of the first transistor according to the data signal (col. 20, line 49 - col. 21, line 8);

a second step of turning off the third transistor and turning on the second transistor (note the second pulse on scanB in fig. 20b), and supplying an amount of charge that causes reduction in the conduction state, set in the first step, of the first transistor (col. 21, lines 22-35); and

vertical scanning in which the n rows of scanning lines are sequentially selected one by one being performed at least twice in one frame period (col. 11, lines 37-42),

wherein, in the first time of vertical scanning, the conduction state of the first transistor of each of the one row of unit circuits coupled to the selected scanning line, among the plurality of unit circuits, is set according to the data signal, and when one of a second set of scanning lines, not included in the first set, is selected, the second transistor of each of the one row of unit circuits coupled to the selected scanning line is turned on to turn off the first transistor (col. 11, lines 37-40), and

wherein, in the second time of vertical scanning, when one of the second set of scanning lines, the conduction state of the first transistor of each of the one row of unit circuits coupled to the selected scanning line is set according to the data signal, and when one of the first set of scanning lines, not included in the second set, is selected, the second transistor of each of the one row of unit circuits coupled to the selected

scanning line is turned on to turn off the first transistor (col. 11, lines 37-40; col. 21, lines 28-32)

Yumoto does not expressly disclose interlaced scanning.

Kanatani discloses, alternating between writing and erasing for even and odd lines (fig. 3).

Kanatani and Yumoto are analogous art because they are both from the same field of endeavor namely electro-optic drive methods.

At the time of the invention it would have been obvious to one of ordinary skill in the art to select the rows and order of operation of Yumoto as taught by Kanatani for the benefit of enhanced display quality (Kanatani; col. 2, line 38 - col. 3, line 4).

Yumoto does not *expressly* disclose that the power-supply lines intersect the m columns of data lines, or that the power-supply lines are connected to the data lines via the capacitor.

Dawson discloses an electro-optical apparatus (fig. 5) comprising, a plurality of power supply lines (VSWP in fig. 4; one for each pixel circuit) that intersect m columns of data lines (data line in fig. 4).

Dawson and Yumoto are analogous art because they are both from the same field of endeavor namely OLED pixel circuitry design.

At the time of the invention it would have been obvious to one of ordinary skill in the art to intersect the data lines with the power supply lines of Yumoto, as taught by Dawson, for the well-known benefit of saving panel space by not requiring an individual power line to each pixel.

Neither Yumoto, Kanatani nor Dawson expressly disclose connecting the power supply line to the data line via the capacitor.

Yamagishi discloses, an electro-optical apparatus (fig. 7) wherein, a power supply line (Vdd in fig. 1) is connected to a data line (data in fig. 1) via a capacitor (C in fig. 1).

Yamagishi, Yumoto and Dawson are analogous art because they are both from the same field of endeavor namely OLED pixel circuitry design.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the pixel circuit of Yumoto with the pixel circuit taught by Yamagishi.

The motivation for doing so would have been to suppress leakage current (Yamagishi; Problem to be Solved).

With respect to claim 37, Yumoto discloses, a method of driving an electro-optical device (fig. 7) the device including:

a plurality of first scanning lines (scanA1-B1 in fig. 7);

a plurality of second scanning lines (scanA2-B2 in fig. 7);

a plurality of third scanning lines (scanA3-B3 in fig. 7);

a plurality of data lines (data in fig. 7);

a plurality of power-supply lines (VSP, VCKB and Vdd in figs. 7 and 19); and

a plurality of unit circuits (25 in fig. 7), each unit circuit including an electro-optical element (OLED in fig. 7), a first transistor having a first terminal, a second terminal, and a first channel region formed between the first terminal and the second terminal (TFT2 in fig. 19), and each unit circuit receiving a first scanning signal supplied through one of

the plurality of first scanning lines (scanA for example in fig. 19) and a second signal supplied through one of the plurality of second scanning lines (scanB for example in fig. 19), each of the plurality of unit circuits further including a capacitor (C in fig. 19), a second transistor (TFT3 in fig. 19) and a third transistor (TFT4 in fig. 19), a second electrode of the capacitor being connected to the one of the plurality of data lines (fig. 19);

the method comprising:

setting a conduction state of the first transistor included in a first set of unit circuits of the plurality of unit circuits that are connected to one of the plurality of first scanning lines, each of the second transistor and the third transistor in the first set of unit circuits being in an on-state during at least a part of a first period in which the setting of the conduction state of the first transistor included in the first set of unit circuits is carried out (figs. 20a-b; col. 20, line 49 – col. 21, line 7);

turning on the second transistor included in the first set of unit circuits of the plurality of unit circuits that are connected to one of the plurality of second scanning lines during at least part of a second period in which the third transistor included in the first set of unit circuits is in an off-state (fig. 20a-b; col. 21, lines 22-41),

the third transistor included in each of the plurality of unit circuits being in an off-state during a fourth period from a first time when the setting of the conduction state of the first transistor included in the first set of unit circuits is completed to a second time when the turning on the second transistor included in a second set of unit circuits

commences (clear from fig. 20a, that the third transistor does not turn on again until all the other rows have been written).

Yumoto has disclosed that the write/extinguish process is applied successively through the display panel. Yumoto has not expressly disclose that the write/extinguish process is applied in a write - row 1; reset - row 2; write - row 3....

Kanatani discloses, alternating between writing and erasing for even and odd lines (fig. 3). Specifically note that this order follows the sequence herein claimed, in that the first line is written, then the second line is erased, then the third line is written.

At the time of the invention it would have been obvious to one of ordinary skill in the art to select the rows and order of operation of Yumoto as taught by Kanatani for the benefit of enhanced display quality (Kanatani; col. 2, line 38 - col. 3, line 4).

To further explain the combination, Yumoto discloses the pixel and transistor operation limitations of the current claim. All that Yumoto does not disclose is the specific order of operations that are claimed. Kanatani discloses an order that fits within the limitations of the order currently claimed.

Neither Kanatani nor Yumoto *expressly* disclose that the power-supply lines intersect the m columns of data lines, or that the power-supply lines are connected to the data lines via the capacitor.

Dawson discloses an electro-optical apparatus (fig. 5) comprising, a plurality of power supply lines (VSWP in fig. 4; one for each pixel circuit) that intersect m columns of data lines (data line in fig. 4).

Dawson, Kanatani and Yumoto are analogous art because they are both from the same field of endeavor namely OLED pixel circuitry design.

At the time of the invention it would have been obvious to one of ordinary skill in the art to intersect the data lines with the power supply lines of Yumoto, as taught by Dawson, for the well-known benefit of saving panel space by not requiring an individual power line to each pixel.

Neither Yumoto, Kanatani nor Dawson expressly disclose connecting the power supply line to the data line via the capacitor.

Yamagishi discloses, an electro-optical apparatus (fig. 7) wherein, a power supply line (Vdd in fig. 1) is connected to a data line (data in fig. 1) via a capacitor (C in fig. 1).

Yamagishi, Yumoto, Kanatani and Dawson are analogous art because they are both from the same field of endeavor namely OLED pixel circuitry design.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the pixel circuit of Yumoto with the pixel circuit taught by Yamagishi.

The motivation for doing so would have been to suppress leakage current (Yamagishi; Problem to be Solved).

With respect to claim 38, Yumoto, Dawson, Yamagishi and Kanatani disclose, the method according to claim 37 (see above).

Yumoto, when combined with Kanatani, Dawson and Yamigishi, discloses, the first scanning signal line being adjacent to the second signal scanning line (Kanatani; fig. 3).

8. Claims 37 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yumoto (US 6,859,193) in view of Miyachi (US 6,937,224) and Dawson et al. (US 6,229,506) and further in view of Yamagishi et al. (JP 2001-147659A)..

With respect to claim 37, Yumoto discloses, a method of driving an electro-optical device (fig. 7), the device including:

a plurality of first scanning lines (scanA1-An in fig. 7);

a plurality of second scanning lines (scanB1-Bn in fig. 7);

a plurality of third scanning lines (scanA3-B3 in fig. 7);

a plurality of data lines (data in fig. 7);

a plurality of power-supply lines (VSP, VCKB and Vdd in figs. 7 and 19); and

a plurality of unit circuits (25 in fig. 7), each unit circuit including an electro-optical element (OLED in fig. 7), a first transistor having a first terminal, a second terminal, and a first channel region formed between the first terminal and the second terminal (TFT2 in fig. 19), and each unit circuit receiving a first scanning signal supplied through of the plurality of first scanning lines (scanA for example in fig. 19) and a second signal supplied through one of the plurality of second scanning lines (scanB for example in fig. 19), each of the plurality of unit circuits further including a capacitor (C in fig. 19), a second transistor (TFT3 in fig. 19) and a third transistor that is controlled by the scanning signal (TFT4 in fig. 19) a second electrode of the capacitor being connected to the one of the plurality of data lines (fig. 19),

the method comprising:

setting a conduction state of the first transistor included in a first set of unit circuits of the plurality of unit circuits that are connected to a one of the plurality of first scanning lines, each of the second transistor and the third transistor in the first set of unit circuits being in an on-state during at least a part of a first period in which the setting of the conduction state of the first transistor included in the first set of unit circuits is carried out (figs. 20a-b; col. 20, line 49 – col. 21, line 7);

turning on the second transistor included in the first set of unit circuits of the plurality of unit circuits that are connected to one of the plurality of second scanning lines during at least part of a second period in which the third transistor included in the first set of unit circuits is in off-state (fig. 20a-b; col. 21, lines 22-41),

the third transistor included in each of the plurality of unit circuits being in an off-state during a fourth period from a first time when the setting of the conduction state of the first transistor included in the first set of unit circuits is completed to a second time when the turning on the second transistor included in a second set of unit circuits commences (clear from fig. 20a, that the third transistor does not turn on again until all the other rows have been written).

Yumoto has disclosed that the write/extinguish process is applied successively through the display panel. Yumoto has not expressly disclose that the write/extinguish process is applied in a write - row 1; reset - row 2; write - row 3....

Miyachi discloses, alternating between writing and erasing for lines (fig. 11a-b). Specifically note that the order of Miyachi follows the sequence herein claimed, in that the first line is written, a second line is reset, then a third line is written.

At the time of the invention it would have been obvious to one of ordinary skill in the art to select the rows and order of operation of Yumoto as taught by Miyachi for the benefit of enhanced display quality (Miyachi; col. 16, lines 4-10).

To further explain the combination, Yumoto discloses the pixel and transistor operation limitations of the current claim. All that Yumoto does not disclose is the specific order of operations that are claimed. Miyachi discloses an order that fits within the limitations of the order currently claimed.

Neither Miyachi nor Yumoto *expressly* disclose that the power-supply lines intersect the m columns of data lines, or that the power-supply lines are connected to the data lines via the capacitor.

Dawson discloses an electro-optical apparatus (fig. 5) comprising, a plurality of power supply lines (VSWP in fig. 4; one for each pixel circuit) that intersect m columns of data lines (data line in fig. 4).

Dawson, Miyachi and Yumoto are analogous art because they are both from the same field of endeavor namely OLED pixel circuitry design.

At the time of the invention it would have been obvious to one of ordinary skill in the art to intersect the data lines with the power supply lines of Yumoto, as taught by Dawson, for the well-known benefit of saving panel space by not requiring an individual power line to each pixel.

Neither Yumoto, Miyachi nor Dawson expressly disclose connecting the power supply line to the data line via the capacitor.

Yamagishi discloses, an electro-optical apparatus (fig. 7) wherein, a power supply line (Vdd in fig. 1) is connected to a data line (data in fig. 1) via a capacitor (C in fig. 1).

Yamagishi, Yumoto, Miyachi and Dawson are analogous art because they are both from the same field of endeavor namely OLED pixel circuitry design.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the pixel circuit of Yumoto with the pixel circuit taught by Yamagishi.

The motivation for doing so would have been to suppress leakage current (Yamagishi; Problem to be Solved).

With respect to claim 39, Yumoto, Yamagishi and Dawson and Miyachi disclose, the method according to claim 37 (see above).

Yumoto, when combined with Miyachi, Yamagishi and Dawson discloses, the first scanning signal line being adjacent to the third scanning signal line (Miyachi; fig. 11b), and the third transistor included in each of the plurality of unit circuits being in an off-state during a fifth period from a third time when the turning on the second transistor included in the second set of unit circuits is completed from a fourth time when the setting of the conduction state of the first transistor included in the third set of unit circuits commences (Miyachi; fig. 19-20b; col. 21, lines 21-41).

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM L. BODDIE whose telephone number is (571)272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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